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Abstract
As the demand increases to build high performance systems, trends in electronic package design have moved toward larger circuit chips, higher number of I/O ports, increased circuit density, and improved reliability. Greater circuit density means increased power density. As the power density is high with 3D technology, the thermal management should be considered carefully in stacked devices.

In the theme, we study the thermal properties of a 3D package proposed by SHARP Corporation by numerical analysis. Several 3D packages, each may have different stacked layers, are considered. Experimental parameters include the channel height, the velocity and the direction of cooling air, and the thickness of air gaps between different layers in the stacked package. In addition, we also study the cooling enhancement techniques by enlarging the gap thickness, inserting heat spreaders and heat sinks into the air gaps, and rearranging the chips placement.

Our simulation results show that inserting heat spreaders and heat sinks into the air gaps can significant reduce the internal thermal resistances of a 3D package. In the cases of inserting heat spreader, the internal thermal resistances are reduced as enlarging the thickness of the heat spreaders. However, the cooling enhancement effect seems to be independent of the thicknesses of the heat sinks. Besides, for a 3D package including several chips with different powers, we propose a systematic method to give a chip placement of better system reliability.
Advisory Committee jing Lee - advisor

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